25.3 On-chip Image Rejection in a Low-IF CMOS Receiver

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A low-IF architecture is suitable for on-chip implementation of RF receivers. However, I/Q phase and amplitude mismatches limit the image-rejection ratio (IRR) of the receiver to 25 to 40dB [1]. In some applications, such as cable modem and cable TV (CATV) tuners, an IRR of 50dB is required. In order to achieve the required IRR in commercial double-conversion TV tuners, an off-chip surface acoustic wave (SAW) filter is typically employed. In this paper, we introduce an adaptive, analog-digital image-reject mixer that improves the IRR to 54dB without any off-chip filters. In this circuit, a complex error signal is generated digitally. The real and imaginary parts of this signal are proportional to the I/Q amplitude and phase mismatches, respectively. This error signal is applied to the phase and amplitude correction blocks in order to correct the mismatches. Test results show that a 54dB IRR is achieved for a single-tone signal. This performance is independent of receiver synchronization and equalization. Therefore, this circuit is effective even in the initialization mode, when synchronization and equalization have not yet converged. No training signal is required, and on-line compensation is possible.

Figure 25.3.1 shows the receiver architecture. It is a double-conversion low-IF receiver, which implements a CATV tuner without SAW filters. In order to prove the concept, the analog portions of the image-reject mixer, along with the phase correction circuitry, were integrated and characterized in a prototype. Other blocks, such as the front-end LNA that has no effect on the image-rejection, were not integrated. The I/Q amplitude mismatch correction and mismatch detection functions are performed in the digital domain, and were realized using non-integrated FPGAs. In the receiver, the desired RF signal is upconverted to 1.1GHz by LO_1, and then quadrature downconverted to 6MHz by LO_2. A 3rd-order, off-chip Bessel LPF is used to filter out the undesired signals. An 8b digitally-controlled phase-shifter (DCPS) is used to correct the I/Q phase mismatches of the resulting low-IF signal. The low-IF signal is digitized using two 10b ADCs. The amplitude mismatch correction is performed in the digital domain as shown in Fig. 25.3.1. It should be mentioned here that, although a completely-digital mismatch compensation technique [2, 3] is typically simpler than an analog approach, a potentially large image signal can saturate the analog blocks when no image cancellation is performed in the analog domain. Furthermore, in a digital compensation technique, a larger ADC dynamic range is required (e.g. 11b ADCs are used in [2] in contrast to the 10b ADCs of this work). Therefore, in some applications, analog-digital or pure-analog mismatch compensation is preferred [1], [4]. After phase and amplitude corrections, two complex digital mixers and filters are used to retrieve the desired and image signals, as shown in Fig. 25.3.1. To detect the mismatches, the received desired signal is multiplied by the received image signal. It can be shown that the resulting product signal has an expected real part (e_ε) that is proportional to the total equivalent amplitude, and an expected imaginary part (e_φ) that is proportional to the total equivalent phase mismatch. These signals are applied to the amplitude and phase correction blocks to compensate the mismatches.

Figure 25.3.2 shows the 8b DCPS. This circuit consists of a gain amplifier (primary cell) in each path (I and Q), along with two multiplying DACs (MDACs) which inject a digitally-controlled leakage signal from one path into the other path as shown in Fig. 25.3.1. Each MDAC has 6 bits realized using 63 equally-weighted, thermometer-controlled secondary cells and 2 additional binary-weighted cells. This configuration has been chosen to guarantee the monotonicity of the input-output characteristics of the DCPS. Monotonicity is important to guarantee the convergence of the compensation loop [1]. By switching M_1 and M_2 in the secondary cell, a signal proportional to V_{in2} (ρV_{in2}) is added to, or subtracted from, the amplified V_{in1} signal (AV_{in1}). If $V_{in1} = \mathrm{Cos}\omega t$ and $V_{in2} = \mathrm{Sin}\omega t$, then the following trigonometric equation shows how an arbitrary phase shift is introduced to V_{in1}:

$$A\mathrm{Cos}(\omega t) \pm \rho \mathrm{Sin}(\omega t) = \sqrt{A^2 + \rho^2}\,\mathrm{Cos}(\omega t \mp \varphi) \qquad (1)$$

where $\varphi = \tan^{-1}(\rho/A)$. The following observations can be made from the DCPS circuit. First, the dc currents of the DCPS are fixed, and switching the secondary cell current does not change any of the bias points. Second, this phase shifter does not introduce any amplitude mismatch to the I and Q signals. Therefore, phase and amplitude compensation loops work independently. Third, this circuit can also be used to correct amplitude mismatch. In this case, V_{in1} and V_{in2} should be both connected to I or Q. Measurements show that the maximum correctable phase mismatch by the DCPS is 18.5°. The accuracy of the phase shifter is 8 bits, which results in an LSB of 0.07° phase shift. As the linearity of the DCPS is important in a CATV application, its IIP3 is measured by applying two equal power tones at 5.5 and 6.5MHz. For a typical input signal power of -25dBm, an IIP3 of 6dBm is required to meet the application requirements. As Fig. 25.3.3 shows, an IIP3 of 8dBm is measured.

The mixers, along with the DCPS, were implemented in a 0.18μm CMOS technology. The digital circuitry was implemented on a FPGA. Two 10b ADCs were used to digitize the low-IF signal. The input signal resides in the TV frequency band (50 to 850MHz). Large mismatches in the setup limit the IRR to 24dB before compensation. However, the IRR is increased to 54dB for a single-tone signal after compensation. Figure 25.3.4 shows the FFT of the digitized, complex low-IF signal ($I + jQ$) after compensation. The low-IF desired and image signals are at 6 and -6MHz, respectively. The performance of the image-reject circuit is also measured for a random 16PAM signal over a 6MHz TV channel. An overall IRR of 53dB is measured as shown in Fig. 25.3.5. The circuit consumes 75mW from a 1.8V supply. 4.3mW is consumed by the MDACs, which were added for phase correction. A comparison with some previously published work is presented in Fig. 25.3.6. Figure 25.3.7 shows a micrograph of the chip. The total and active areas are 2.25mm² and 0.57mm², respectively.

References:

[1] L. Der and B. Razavi, "A 2-GHz CMOS Image-Reject Receiver with LMS Calibration," *IEEE J. Solid-State Circuits,* vol. 38, no. 2, pp. 167-175, Feb., 2003.

[2] C. H. Heng et al., "A CMOS TV Tuner/Demodulator IC with Digital Image Rejection," *IEEE ISSCC Dig. Tech. Papers,* pp. 432-433, Feb., 2005.

[3] L. Yu and M. Snelgrove, "A Novel Adaptive Mismatch Cancellation System for Quadrature IF Radio Receivers," *IEEE T. CAS-II,* vol. 46, no. 6, pp. 789-801, June, 1999.

[4] J. V. Sinderen et al., "A 48-860MHz Digital Cable Tuner IC with Integrated RF and IF Selectivity," *IEEE ISSCC Dig. Tech. Papers,* pp. 444-445, Feb., 2003.

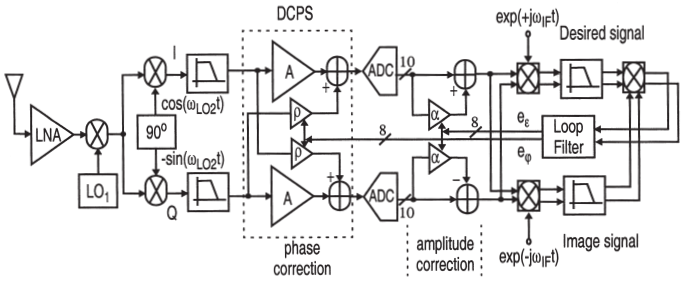

Figure 25.3.1: The receiver architecture.

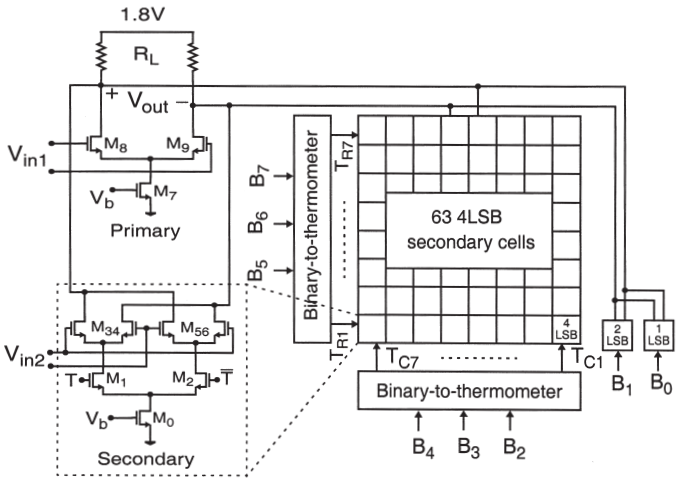

Figure 25.3.2: The 8b DCPS circuit.

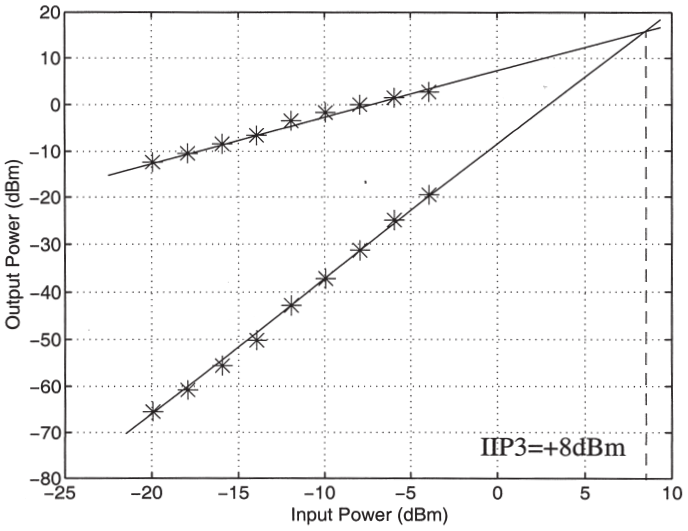

Figure 25.3.3: Measured IIP3 of the DCPS.

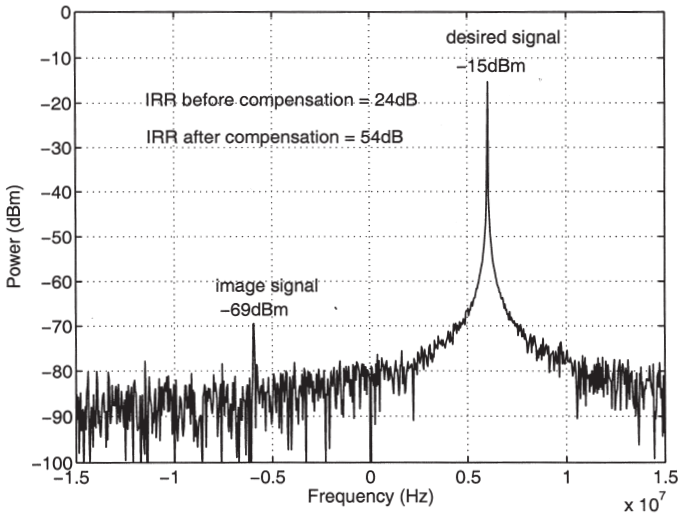

Figure 25.3.4: FFT of the digitized low-IF signal after compensation.

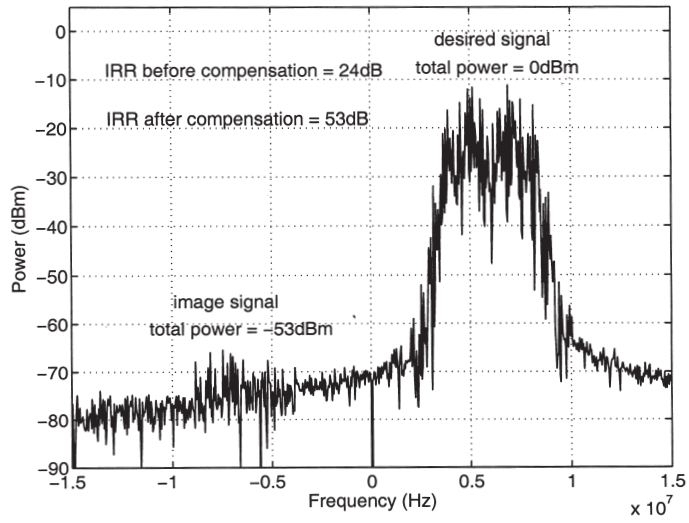

Figure 25.3.5: IRR over the bandwidth of a TV channel for a 16PAM signal.

Work	*Compensation*	*Comments*
This work	Analog-Digital	- A training signal is not required. - On-line compensation is possible. - An 8-bit DCPS is used.
Der, JSSC03	Analog-Digital	- A training signal is required. - On-line compensation is not possible. - An 11-bit DAC is used.
Heng, ISSCC05	Digital	- Not suitable for applications with a large image signal. - Large dynamic range required for ADCs (11 bits). - More power because of high-resolution ADCs.
Sinderen, ISSCC03	Analog	- RF and IF polyphase filters for out-of-band image rejection. - In-band image rejection relies on I/Q path matching. - Not amenable to migration across process corners and temperature variations. - More power because of switchable filters.

Figure 25.3.6: Comparison with previously published work.

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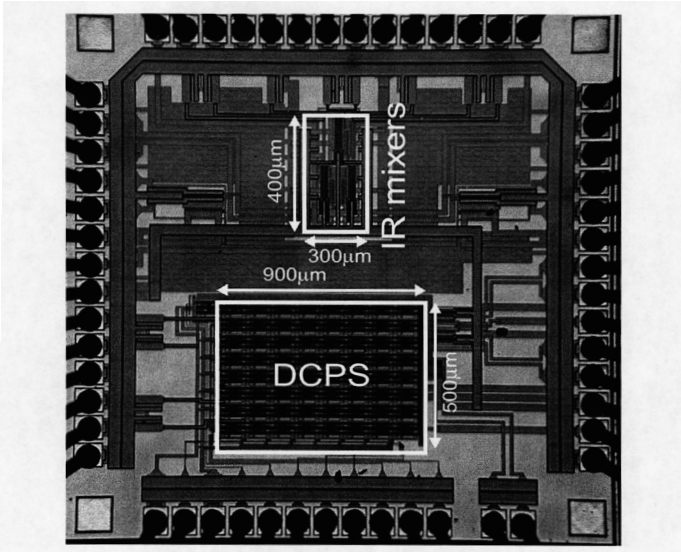

Figure 25.3.7: Chip micrograph.

